METHOD FOR EVALUATING AN INTEGRATED ELECTRONIC DEVICE

ABSTRACT OF THE DISCLOSURE

The structure allows checking an integrated electronic device comprising an oxide layer to be measured located above a doped pocket of a wafer of doped semiconductor material and arranged adjacent to a gate region of polycrystalline semiconductor material. The structure is formed at a suitable point of the wafer and comprises an oxide test region of the same material, having the same thickness and the same electrical characteristics as the oxide layer to be measured and a polycrystalline region of the same material, having the same thickness and the same electrical characteristics as the gate region. The polycrystalline region extends preferably along the perimeter of a square and delimits laterally the oxide test region, the area of which is greater than the area of the oxide layer to be measured so as to allow non-destructive testing, on-line, of the oxide layer to be measured during an early stage of the manufacturing process.